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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,458	06/01/2001	Joshua M. Conner	068354.1439	8446

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,458	CONNER ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/10/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 19-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 19-34 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/4/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim19 is objected to because of the following informalities: In line 3, please change "produces" to "produce". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 24, 25, and 29-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 24 recites the limitation "the shift increment" in line 1. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 25 recites the limitation "the shift increment" in line 1. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 29 recites the limitation "the operand" in lines 21 and 22. There is insufficient antecedent basis for this limitation in the claim. Claims 30-34 are rejected for incorporating the defects of claim 29.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 19-28 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

9. The language of the claims raises a question as to whether the claims are directed merely to an abstract idea that is not tied to a technological art, environment or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101. See Gottschalk v. Benson, 409 U.S. 63 (1972) and In re Benson and Tabbot, 169 USPQ 548 (CCPA 1971).

10. Mental processes and abstract intellectual concepts are not patentable as they are the basic tools of scientific and technological work. Claims 19-28 merely claim a method of shifting and concatenating values to produce a result, or the manipulation of an abstraction. See claim 8 in Gottschalk v. Benson, 409 U.S. 63 (1972).

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 19-26 and 28 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual (herein after Intel).

13. Referring to claim 19, Intel has taught a method of shifting a multi-word value comprising:

a. performing a first shift operation on a first portion of the multi-word value to produces one or more overflow bits (Pages 4-16 and 4-17, Bits are shifted out of the source register.);

b. performing a second shift operation on a second portion of the multi-word value,

c. where the second shift operation comprises:

i. producing a shift result; and concatenating the shift result and the overflow bits (Pages 4-16 and 4-17, A lower portion of bits of the destination are concatenated with the bits shifted out of the source register.).

14. Referring to claim 20, Intel has taught the method of claim 19, where the second shift operation is a multi-precision shift instruction, and where the second shift operation produces a result, the method further comprising:

a. fetching and decoding the multi-precision shift instruction (Page 18-7, First paragraph, Instructions are inherently fetched and decoded in the processing system, Pages 4-16 and 4-17, SHLD and SHRD); and

b. outputting the result (Pages 4-16 and 4-17, The result is stored back into, or output to the destination operand.).

15. Referring to claim 21, Intel has taught the method of claim 20, as described above, and where the multi-precision shift instruction is a shift left instruction (Page 4-16, SHLD).

16. Referring to claim 22, Intel has taught the method of claim 20, as described above, and where the multi-precision shift instruction is a shift right instruction (Pages 4-16 and 4-17, SHRD).

17. Referring to claim 23, Intel has taught the method of claim 20, as described above, and where the multi-precision shift instruction specifies a shift increment (Page 4-16, The CL register or an immediate byte in the instruction specifies the number of bits to be shifted.).

18. Referring to claim 24, Intel has taught the method of claim 20, as described above, and where the shift increment is greater than or equal to the number of bits in a word (Page 4-19).

19. Referring to claim 25, Intel has taught the method according to claim 20, as described above, and where the shift increment is less than the number of bits in a word (Pages 4-16, 25-289 to 25-290).

20. Referring to claim 26, Intel has taught the method of claim 19, as described above, and further comprising:

a. storing one or more bits shifted out of the second portion of the multi-word value during the second shift instruction in a carry register (Pages 4-16 and 4-17, CF).

21. Referring to claim 28, Intel has taught the method of claim 19, as described above, and further comprising:

a. storing one or more of the overflow bits in a carry register (Pages 4-16 and 4-17).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 27 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual (herein after Intel), in view of Silverbrook, US Patent 6,314,200.

24. Referring to claim 27, Intel has taught the method of claim 19, as described above. Intel has not specifically taught all of the logical operations required to implement the shift instructions. Specifically, Intel has not taught where concatenating the shift result and the overflow bits comprises: performing a logical OR operation on at least one bit in the shift result and at least one overflow bit. However, Silverbrook et al. have taught performing a logical OR operation on at least one bit in a shift result and at least one overflow bit (column 222, lines 10-24) in order to implement multiple precision shifting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Intel, include performing the claimed OR operation, as taught by Silverbrook et al., for the desirable purpose of implementing multiple precision shifting (column 222, lines 10-24).

25. Referring to claim 29, Intel has taught a processor for processing multi-precision shift instructions, comprising:

a. a program memory for storing instructions including at least one multi-precision shift instruction (Page 3-2, lines 1-3);

b. a program counter for identifying current instructions for processing (Page 3-15, section 3.3.5, Instruction Pointer), and

c. a barrel shifter for executing shift instructions (Page 4-16 and 4-17), including the at least one multi-precision shift instruction (Pages 4-16 and 4-17, SHLD and SHRD), the barrel shifter including:

i. one or more carry registers for storing values shifted out of sections of the barrel shifter (Page 4-16 and 4-17, CF); and logic for concatenating values stored in one or more carry registers with values in the barrel shifter (pages 25-289 to 25-292); and

d. where the barrel shifter is operable to shift a multi-word value (Pages 4-16 and 4-17, SHLD and SHRD shift doubleword operands), and where when shifting a multi-word value the barrel shifter:

i. executes at least one shift instruction to:

(1) load a first operand into a section within the barrel shifter, where the first operand is a first portion of the multi-word value (Pages 4-16 and 4-17, The source operand is loaded into the source register.); and

(2) generate one or more overflow bits (Pages 4-16 and 4-17, Bits are shifted out of the source register.); and

e. executes at least one multi-precision shift instruction fetched from the program memory (Pages 4-16 and 4-17, The SHRD and SHLD instruction are executed.) to:

i. load a second operand into a section within the barrel shifter, where the second operand is a second portion of the multi-word value (Pages 4-16 and 4-17, The destination operand is loaded into the destination register.);

ii. shift the operand; concatenate the operand with one or more of the overflow bits (Pages 4-16 and 4-17, A lower portion of bits of the destination are concatenated with the bits shifted out of the source register.); and

ii. output the shifted value (Pages 4-16 and 4-17, The result is stored back into, or output to the destination operand.).

26. Intel has not specifically taught all of the hardware logic required to implement the shift instructions. Intel has not specifically taught OR logic for concatenating values stored in the one or more carry registers with values in the barrel shifter. Silverbrook et al. have taught OR logic for concatenating values stored in carry registers with values in the barrel shifter (column 222, lines 10-24) in order to implement multiple precision shifting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Intel, include the claimed OR logic, as taught by Silverbrook et al., for the desirable purpose of implementing multiple precision shifting (column 222, lines 10-24).

27. Claims 30-34 do not recite limitations above the claimed invention set forth in claims 11-15 and are therefore rejected for the same reasons set forth in the rejection of claims 11-15 above.

Response to Arguments

28. Examiner notes that Applicant has not provided any arguments from which to respond.

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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